Claims

[c1] What is claimed is:

1.A microprocessor apparatus comprising:

a program counter for storing a program count value;

a processing unit coupled to the program counter comprising:

(a) an instruction fetching means coupled to the program counter for reading program instructions according to the program count value and storing fetched instructions in a buffer;

(b) an instruction decoding means coupled to the instruction fetching means for decoding and dispatching buffered instructions for execution;

a read only memory coupled to the processing unit for storing afirst program;

an auxiliary programmable-memory coupled to the processing unit for storing patches to replace corresponding instructions in the first program along with a table containing a replacement program count value for each patch; and

a controller coupled to the program counter and the processing unit for passing an indirect branch instruction corresponding to one of the patches to the process-

ing unit in response to a match between the program count value and aninitializing program count value, wherein the indirect branch instruction will insert the replacement program count value corresponding to the match into the program counter.

[c2] 2.The microprocessor apparatus in claim 1 wherein the controller further comprises:
a register for storingthe initializing program count value.

[c3] 3.A method for executing patch program segments in lieu of corresponding parts in a first program comprising:
(a)comparinga program count value of a program counter with aninitializing program count value;
(b)inserting an indirect branch instruction with an index into a buffer of an instruction fetching means when a match is made in step (a);
(c)accessing a table in an auxiliary programmable memory according to the index of the indirect branch instruction; and
(d)changing the program count value of the program counter according to the table entry.

[c4] 4.The method in claim 3 further comprising:
(e)ending the patch with a terminating instruction branch.

[c5] 5.The method in claim 4 further comprising:
branching back to the first program in the read only memory with the terminating branch instruction.